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| **EWULogo.png** | **EAST WEST UNIVERSITY** |
| **Department of Computer Science and Engineering** |
| **B.Sc. in Computer Science and Engineering Program** |
| **Assignment I, Spring 2021 Semester** |

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| **Course:** | **CSE 360 Computer Architecture, Section-1 & 2** |
| **Instructor:** | **Ahmed Wasif Reza, PhD, Associate Professor, CSE Department** |
| **Full Marks:** | **20 (5×4=20)** |
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1. We want to compare the computers C1 and C2. C1 has the machine instructions for the floating-point operations, while C2 has not (FP operations are implemented in the software using several non-FP instructions). Both computers have a clock frequency of 500 MHz. In both we perform the same program, which has the following mixture of commands:

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| **Command Type** | **Dynamic Share of instructions in program** | **Instruction duration** |  |
|  |  | **C1** | **C2** |
| FP addition | 16% | 6 | 20 |
| FP multiplication | 10% | 8 | 32 |
| FP division | 8% | 10 | 66 |
| Non - FP instructions | 66% | 3 | 3 |

1. Calculate the MIPS for the computers C1 and C2.
2. Calculate the CPU program execution time on the computers C1 and C2, if there are 24000 instructions in the program?
3. At what mixture of instructions in the program will both computers C1 and C2 be equally fast?
4. A program runs in 300 seconds on a machine, with division operations responsible for 160 seconds. You want to improve the speed of the program to run 3 times faster. How much do you have to improve the speed of the division operations? Illustrate the whole process.
5. Consider a 32-bit microprocessor. Assume that, on average, 20% of the operands and instructions are 64 bits long, 40% are 32 bits long, and 40% are 16 bits long.
6. Is it possible to double the performance using 64-bit microprocessor having the same bus cycle duration of a 32-bit microprocessor?
7. Design the whole process.
8. Assume that a computer has L1 cache with miss ratio of 5% and access time of 1ns, L2 cache with hit ratio of 99% and access time of 10ns, main memory with hit ratio of X% and access time of 50ns.
9. What should be the value of X if the effective access time is not more than 1.5ns?
10. Design the system.
11. A computer system uses 16-bit memory addresses. It has a 2K-byte cache organized in a direct-mapped manner with 64 bytes per cache block. Assume that the size of each memory word is 1 byte. Show the number of bits in each of the Tag, Block, and Word fields of the memory address and design the cache organization.